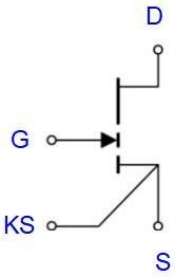
Description

SGN65N130DN is an enhancement mode GaN-on-silicon transistor. GaN is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero.

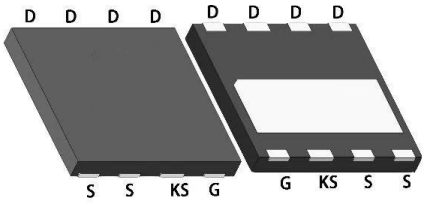
Features

- 650 V enhancement mode power switch
- $R_{DS(on)}$ =130mΩ
- $I_{DS(max)}$ = 15A
- Easy gate drive requirements (0 V to 6 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Zero reverse recovery loss

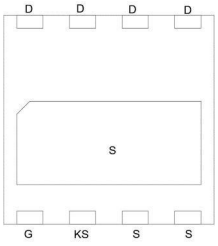


Device Information

Part Number	Marking Code	Package	Packing
SGN65N130DN	SGN65N130	DFN8×8	260pcs/tray



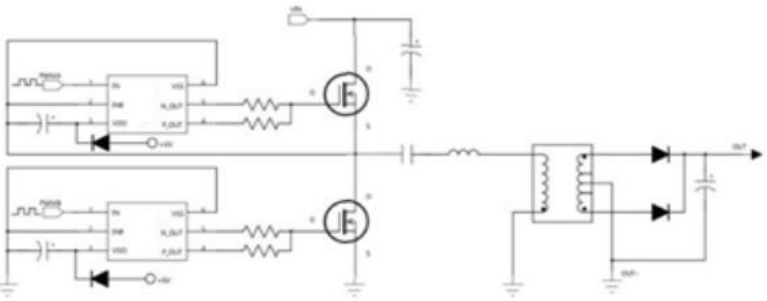
SGN65N130DN DFN8x8



SGN65N130DN Bottom View

Applications

- Fast Battery Charging
- LED lighting drivers
- Power Factor Correction
- LLC Converters
- Wireless Power Transfer



Typical application circuit for LL

Absolute Maximum Ratings (Tc=25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-7 to 6	V	
Continuous drain current*	I_D	18	A	Tc=25℃
		14	A	Tc=125℃
Operation and storage temperature	T_j	-55 to 150	℃	
	T_{stg}	-55 to 150	℃	

*** An Estimated Value**

Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}	60.3	°C/W	
Thermal resistance, junction-case	R_{thJC}	1.1	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	℃	MSL3

Electrical Characteristics (Tc=25℃ unless otherwise specified)

Typical Performance – Static

Parameter	Symbol	Values			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown voltage	BV_{DS}	650	/	/	V	VGS=0V, ID=20μA
Total drain leakage current	I_{DSS}	/	0.7	25	μA	VDS=650V, VGS=0V, Tj=25℃
		/	6	200	μA	VDS=650V, VGS=0V, Tj=150℃
Gate-to-source current	I_{GSS}	/	66	/	μA	VDS=0V, VGS=6V, Tj=25℃
Static drain-source on-resistance	$R_{DS(ON)}$	/	104	130	mΩ	VGS=6V, ID=3A, Tj=25℃
		/	215	/	mΩ	VGS=6V, ID=3A, Tj=150℃
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	VDS=VGS, ID=3.5mA,

Typical Performance – Dynamic

Parameter	Symbol	Values			Unit	Test condition
		Min	Type	Max		
Input capacitance	C_{ISS}	/	119	/	pF	V_{DS}=400V, V_{GS}=0V, f=1MHz
Output capacitance	C_{OSS}	/	39	/	pF	
Reverse transfer Capacitance	C_{RSS}	/	0.3	/	pF	
Output capacitance, energy Related	$C_{OSS(er)}$	/	48	/	pF	V_{DS}=0V to 400V,V_{GS}=0V
Output capacitance time related	$C_{OSS(tr)}$	/	78	/	pF	
Total gate charge	Q_G	/	3.7	/	nC	V_{DS}=400V, V_{GS}=0V to 6V
Gate-drain charge	Q_{GD}	/	1.4	/	nC	
Gate-source charge	Q_{GS}	/	0.2	/	nC	
Gate Resistance	R_G	/	3.3	/	Ω	*f* = *f*res, Open drain

Characteristic Curve

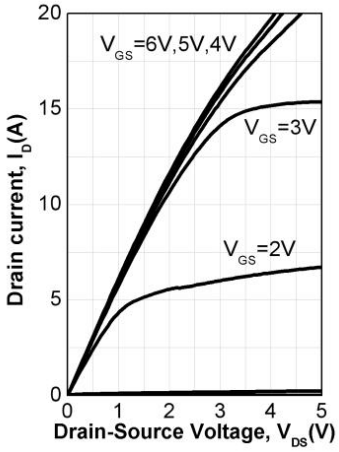


Fig.1 Typical output characteristics @ Tj=25℃

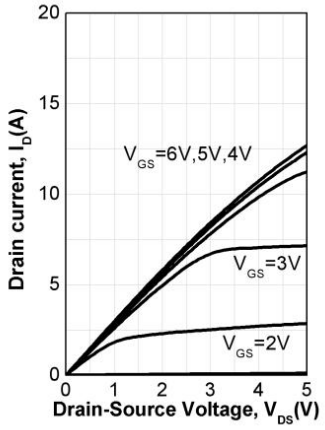


Fig.2 Typical output characteristics @ Tj=150℃

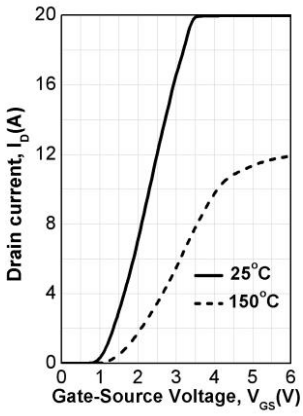


Fig.3 Typical transfer characteristics @ VDS=5V

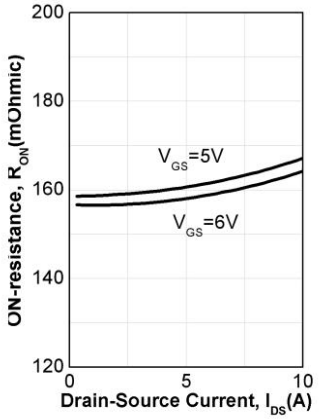


Fig.4 ON-resistance for various drain current @ 25℃

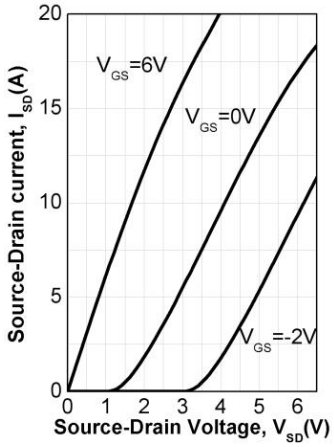


Fig.5 Typical reverse conduction characteristics

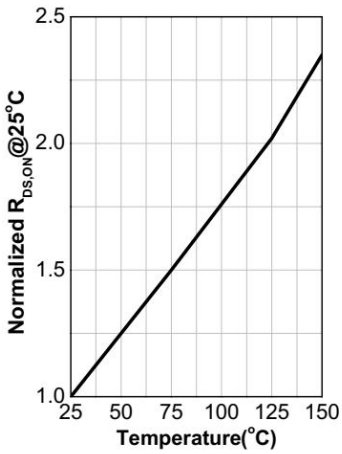
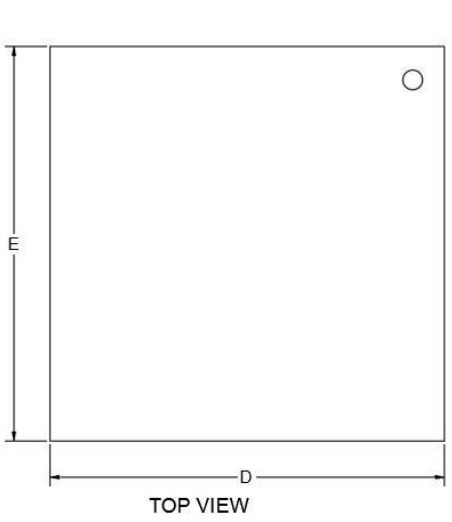


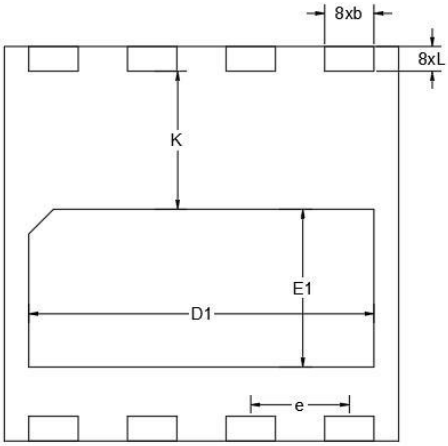
Fig.6 Normalized ON-resistance at various temperatures

Package

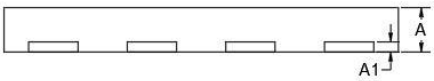
Dimensions(mm)			
Symbol	**Min.**	**Nom.**	**Max.**
A	0.80	0.90	1.00
A1		REF 0.203	
B	0.95	1.00	1.05
D	7.90	8.00	8.10
D1	6.90	7.00	7.10
E	7.90	8.00	8.10
E1	3.10	3.20	3.30
E		REF 2.00	
K		REF 2.80	
L	0.45	0.50	0.55



TOP VIEW



BOTTOM VIEW



SIDE VIEW

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