Description

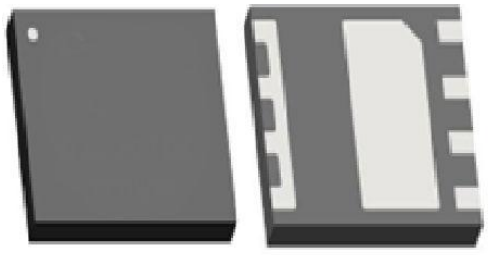
SGI65N200DFDF is an integrated device that includes a single channel high speed driver and an enhanced GaN transistor which is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero.

Features

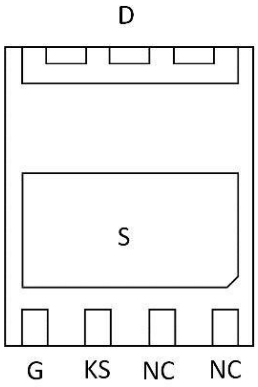
- 650 V enhancement mode power switch
- RDS(on) =200mΩ
- IDS(max) = 10A
- Easy gate drive requirements (0 V to 6 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Zero reverse recovery loss

Device Information

Part Number	Marking Code	Package	Packing
SGI65N200DFDF	SGI65N200DF	DFN5×6	4000pcs/reel



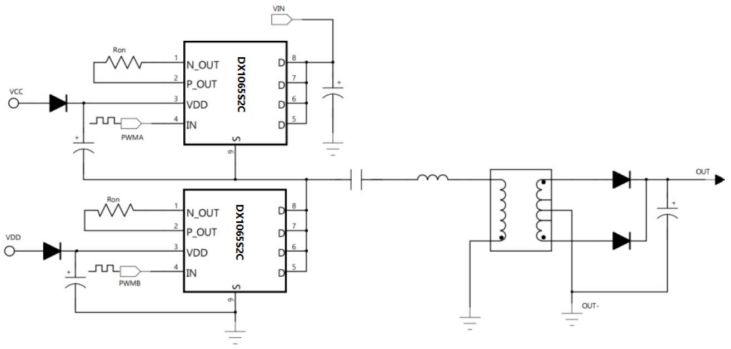
SGI65N200DFDF DFN5x6



SGI65N200DFDF Bottom View

Applications

- Fast Battery Charging
- LED lighting drivers
- Power Factor CorrectionL
- LLC Converters
- Wireless Power Transfer



Typical application circuit for LLC

Absolute Maximum Ratings (Tc=25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-10 to 6	V	
Continuous drain current*	I_D	10	A	Tc=25℃
		4.5	A	Tc=125℃
Operation and storage temperature	T_j	-55 to 150	℃	
	T_{stg}	-55 to 150	℃	

*** An Estimated Value**

Electrical Characteristics (Tc=25℃ unless otherwise specified) Typical

Performance – Static

Parameter	Symbol	Values			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown voltage	B_{VDS}	650	/	/	V	VGS=0V, ID=20μA
Total drain leakage current	I_{DSS}	/	1	10	μA	VDS=650V, VGS=0V, Tj=25℃
		/	8	110	μA	VDS=650V, VGS=0V, Tj=150℃
Gate-to-source current	I_{GSS}	/	10	/	μA	VDS=0V, VGS=6V, Tj=25℃
Static drain-source on-resistance	$R_{DS(ON)}$	/	150	200	mΩ	VGS=6V, ID=3A, Tj=25℃
		/	300	/	mΩ	VGS=6V, ID=3A, Tj=150℃

Single Channel High Speed Drive Key Technical Indicators

Absolute Maximum Ratings

Over operating free-air temperature range(Unless otherwise noted) (1)

Description	Min	Max	Unit
VDD to VSS	-0.3	5.5	V
IN, INB to VSS	-0.3	20	V
N_OUT to VSS	-0.3	VDD+0.3	V
P_OUT to VSS	-0.3	VDD+0.3	V
Junction temperature		+150	℃
Storage temperature	-55	+150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating conditions

Over operating free-air temperature range(Unless otherwise noted)

Description	Min	Max	Unit
VDD	4.2	5.2	V
IN, INB	4.0	18	V
Operating temperature	-20	+125	℃

Electrical Characteristics

The maximum and minimum limits are determined by design, test, or data correlation. The typical values represent the most likely parametric norm at TJ = 25 ℃ for reference purposes only. (unless otherwise specified, VDD = 5V).

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	VDD operating voltage	Tj range of -20℃ to 125℃	4.7	5.0	5.2	V
UVLO	VDD undervoltage lockout	VDD rising	3.8	4.0	4.2	V
	VDD undervoltage lockout hysteresis			0.1		V
	VDD undervoltage lockout to output delay time			1300		ns
I_{LK-N}	Output leakage current	N_OUT=VDD		0.5	15	μA
I_{LK-P}	Output leakage current	P_OUT=VDD		0.5	15	μA
N Channel output						
R_{ON-N}	Drive output resistance - pulling down	VDD=5V			0.36	Ω
P Channel output						
R_{ON-P}	Drive output resistance – pulling up	VDD=5V		1.62	1.64	Ω
Logic input						
V_{IH}	Input voltage - logic 1		2.05			V
V_{IL}	Input voltage - logic 0				1.78	V

High frequency characteristics

Over operating free-air temperature range (unless otherwise noted)

Symbol	Description	Test conditions	Min	Typ.	Max.	Unit
t_R	Rise time1)	CL = 1000 pF		5.2		ns
t_F	Fall time	CL = 1000 pF		3.3		ns
t_{D-ON}	Turn-on propagation delay	CL = 1000 pF		6.3		ns
t_{D-OFF}	Turn-off propagation delay	CL = 1000 pF		6.3		ns

(1) The rise time is the time required for the output signal to rise from 10% to 90%.

(2) The fall time is the time required for the output signal to drop from 90% to 10%.

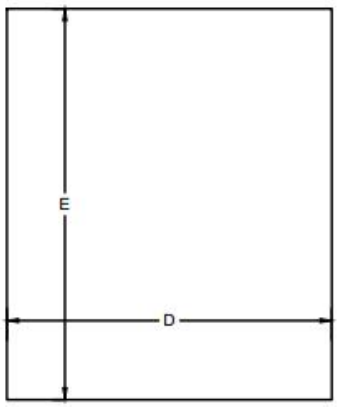
(3) The on propagation delay is the time required for the input signal to rise to 50% and the output signal to rise to 10%.

(4) The turn off propagation delay is the time required for the input signal to drop to 50% and the output signal to drop to 10%.

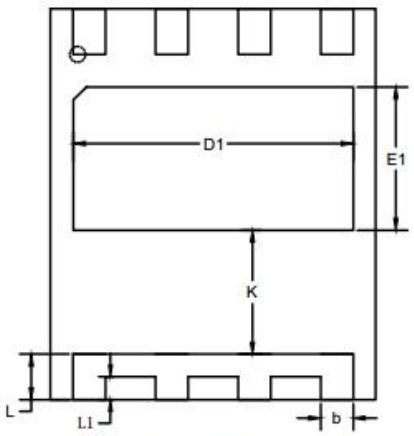
Package Outline Dimensions

DFN5x6

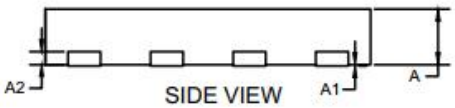
Dimensions(mm)			
Symbol	**Min.**	**Nom.**	**Max.**
A	0.8	0.85	0.9
A1		0.02	0.05
A2		0.2(REF)	
b	0.45	0.50	0.55
D	4.90	5.00	5.10
D1	4.20	4.30	4.40
E	5.90	6.00	6.10
E1	2.10	2.20	2.30
e		1.27	
k	1.9	-	-
L	0.65	0.7	0.75



TOP VIEW



BOTTOM VIEW



SIDE VIEW

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